REMARKS

Claims 1-24 remain in the application. By this amendment claims 1, 12, 14, 19-22, and 24 have been amended and claims 2-11, 13, 15-18, and 23 remain in original form. Claims 25-29 were canceled without prejudice in response to a requirement for restriction.

The specification has been amended to correct a typographical error.

REJECTION OF CLAIM 24 UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

Claim 24 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. This rejection is respectfully traversed.

Claim 24 has been amended to more particularly point out and distinctly claim the subject matter which applicant regards as the invention. Accordingly, claim 24 is believed to be in condition for allowance, which action is earnestly solicited.

REJECTION OF CLAIMS 1-11, 13-16, 19, AND 20 UNDER 35 U.S.C. § 102(b)

Claims 1-11, 13-16, 19, and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Iwamatsu et al., U.S. Patent No. 5,905,286. This rejection is respectfully traversed.

Iwamatsu et al. teach in column 37, lines 1-17, that as shown in FIG. 151, gate electrodes 6 are formed on SOI layers 3 with gate oxide films 50 therebetween, and then side wall oxide films 13 are formed in contact with the opposite surfaces of each gate electrode 6. After forming metal silicide layers 8 on gate electrodes 6 and source/drain regions of SOI layers 3, interlayer insulating film 9 is formed over the whole surface. Contact holes are formed at predetermined regions of interlayer insulating film 9. Interconnection layers 10 filling the contact holes are formed. The gate electrode 6 is formed of a polycrystalline silicon layer containing phosphorus at an impurity region not lower than $1x10^{20}/cm^2$.

Iwamatsu et al. further teach in column 37, lines 43-59, that as shown in FIG. 158, resist 102 is formed over the PMOS region. Using resist 102 and nitride film 4a at the NMOS region as a mask, boron ions are implanted into the side portions of SOI layer 3 at the NMOS region by the continuous rotary implantation method with the implantation energy of 30-40 keV and the implantation concentration of $3x10^{13}$-$15x10^{13}/cm^2$. Thereby, isolation regions 3a are formed. Thereafter, resist 102 is removed. After removing nitride films 4a and oxide films 5, gate oxide films 50 are formed again on the upper surfaces of SOI layers 3 as shown in FIG. 159. Thereafter, a process similar to the manufacturing process of the twenty-sixth embodiment already described with reference to FIG. 151 is performed to form the structure shown in FIG. 160. FIG. 161 is a plan showing a structure in FIG. 160, and FIG. 160 is a cross section taken along line 300-300 in FIG. 161. FIG. 162 is a cross section taken along line 400-400 in FIG. 161.

Iwamatsu et al. teach in column 17, lines 28-67, and continuing to column 18, lines 1-18, source drain regions 3b and 3c having an LDD structure are formed at SOI layer 3 in the NMOS region and are spaced by a predetermined distance with a channel region 3d therebetween. An impurity implanted region 3a for raising a threshold voltage of a parasitic transistor is formed at the vicinity of a side surface of SOI layer 3 at the NMOS region. A gate electrode 6 is formed on channel region 3d with a gate oxide film 50 therebetween. Side wall insulating films 13 are also formed in contact with side surfaces of gate electrode 6. A titanium silicide film 8a is formed over the surfaces of source/drain regions 3b and 3c and the surface of gate electrode 6 for reducing resistance.

Source drain regions 3e and 3f having an LDD structure are formed at SOI layer 3 in the PMOS region and are spaced by a predetermined distance with a channel region 3g therebetween. Side wall insulating films 13 are formed in contact with side surfaces of SOI layer 3. Side wall insulating films 13 are formed in contact with side surfaces of SOI layer 3. A gate electrode 6 is formed on channel region 3g with gate oxide film 50 therebetween. Side wall insulating films 13 are formed in contact with side surfaces of gate electrode 6. Titanium silicide film 8a is formed over the surfaces of source/drain regions 3e and 3f and the surface of gate electrode 6 for reducing resistance. The upper portions of each SOI layer 3 are rounded. Thereby, it is possible to prevent concentration of an electric field at the upper side portions of SOI layers 3. Consequently, lowering of

a threshold voltage of a parasitic transistor can be prevented, which suppresses turn-on of the parasitic transistor. As a result, subthreshold characteristics of a regular MOS transistor are prevented from being adversely affected by the parasitic transistor. The lower portion of the side surface of SOI layer 3 extends substantially perpendicularly to a main surface of the buried oxide film 2, so that such a structure can be prevented that a thin portion is formed at the lower side portion of SOI layer 3. Thereby, it is possible to prevent lowering of the threshold voltage of parasitic transistor which may be caused by reduction of the thickness of SOI layer 3 at the vicinity of its side surface.

In this first embodiment, buried oxide film 2 is provided at its main surface with a U-shaped concavity 2a, which is located at a region between SOI layers 3 at the NMOS and PMOS regions. Concavity 2 has a rounded portion at and near its open end. Thereby, it is possible to prevent effectively remaining of etching residue near the lower side portions of SOI layers 3, which may be caused by the fact that the lower portion of side surface of SOI layer 3 extends perpendicularly.

An interlayer oxide film 9 is formed over SOI layers 3 and gate electrodes 6. Interlayer oxide film 9 is provided at predetermined regions with contact holes 9a, 9b, 9c and 9d. There are formed interconnections 10a, 10b, 10c and 10d which have portions located in contact holes 9a-9d and electrically connected to source/drain regions 3b, 3c, 3e and 3f, respectively.

Iwamatsu et al. teach in column 18, lines 55-67, and continuing to column 19, lines 1-16, a polycrystalline silicon film 11 having a thickness of about 50 Å-500 Å is formed over nitride films 4a and 4b and SOI layer 3 by the low pressure CVD method. Polycrystalline silicon film 11 is oxidized in a wet atmosphere under the temperature condition of 950 °C as shown in FIG. 7. In this processing, conditions are determined to oxidize entire polycrystalline silicon film 11. During oxidation of polycrystalline silicon film 11, when polycrystalline silicon film 11 on buried oxide film 2 and polycrystalline silicon film 11 on nitride films 4a and 4b are entirely oxidized, the oxide film in these regions does not extend any longer. However, side portions of SOI layer 3 are further oxidized even after regions of polycrystalline silicon film 11 which are in contact with the side surfaces of SOI layer 3 are entirely oxidized. Thereby, as shown in FIG. 8, each upper side portion of SOI layer 3 is rounded, and the lower portion of each side surface

extends substantially perpendicularly to the main surface of buried oxide film 2. These portions are covered with oxide film 12. More specifically, since polycrystalline silicon film 11 is formed also on the surface of buried oxide film 2, oxidation of polycrystalline silicon film 11 on buried oxide film 2 consumes oxidant which tends to move up to a rear surface of SOI layer 3 during oxidation of polycrystalline silicon film 11. Thereby, it is possible to prevent movement of oxidant up to the lower surface of SOI layer 3, and thus oxidation of the rear surface of SOI layer 3 can be prevented. Thereby, the lower portion of side surface of SOI layer 3 extends substantially perpendicularly to the main surface of buried oxide film 2.

Iwamatsu et al. teach in column 19, lines 59-66, that shown in FIG. 14 is a gate oxide film 50 formed over SOI layer 3 and concavity 2a. Polycrystalline silicon layer 6 which contains a large amount of phosphorus and having a thickness of about 2000 Å is formed over gate oxide film 50. A resist 105 is formed at predetermined regions on polycrystalline silicon layer 6. Using resist 105 as a mask, polycrystalline silicon layer 6 is anisotropically etched to form gate electrodes 6 of a form shown in FIG. 15.

Iwamatsu et al. teach in column 20, lines 19-27, that as shown in FIG. 18, a low pressure CVD method is performed to form oxide film 13 having a thickness of about 1500 Å and covering the whole surface. Oxide film 13 is anisotropically etched to form side wall oxide films 13 which are in contact with the opposite side surfaces of gate electrodes 6 as shown in FIG. 19. Side wall oxide films 13 remain also on the opposite side surfaces of SOI layer 3. Thereafter, a sputtering method is performed to form titanium layer 8 having a thickness of about 200 Å.

Iwamatsu et al. further teaches in column 20, lines 55-61, that as shown in FIG. 22, an interlayer oxide film 9 having a thickness of about 7000 Å is formed over the whole surface, and then resist 110 is formed at predetermined regions on interlayer oxide film 9. Using resist 110 as a mask, interlayer oxide film 9 is anisotropically etched to form contact holes 9a, 9b, 9c and 9d located above source/drain regions 3b, 3c, 3e and 3f, respectively.

Iwamatsu et al. further teach in column 35, lines 49-67, and continuing to column 36, lines 1-22, a twenty-fifth embodiment having a purpose of removing fixed charges existing at an interface between SOI layer 3 and buried oxide film 2. Existence of fixed

charges may cause generation of a parasitic transistor. Therefore, generation of the parasitic transistor can be suppressed by removing fixed charges. More specifically, if SOI layer 3 is formed on buried oxide film 2 formed on silicon substrate 1 as shown in FIG. 140, fixed charges exist at the interface between SOI layer 3 and buried oxide film 2. In this case, a silicon oxide film 71 is formed at a predetermined region on the main surface of SOI layer 3 as shown in FIG. 141, and then SOI layer 3 is patterned using silicon oxide film 71 as a mask. Thereafter, silicon oxide film 71 is removed by wet etching. By the wet etching for removing silicon oxide film 71, undercut portions are formed at buried oxide film 2 as shown in FIG. 142. Thereby, buried oxide film 2 has a convexity 2a. Thereafter, SOI layer 3 is oxidized in a wet atmosphere at 1100 °C or more to form an oxide film 72 as shown in FIG. 143. Formation of oxide film 72 rounds off the corners of SOI layer 3, and can remove the fixed charges existing between convexity 2a of buried oxide film 2 and SOI layer 3. Since convexity 2a of buried oxide film 2 is only in slightly contact with SOI layer 3, oxidation of SOI layer 3 does not cause a stress between SOI layer 3 and convexity 2a of buried oxide film 2.

As shown in FIG. 144, a silicon oxide film 73 is formed on the whole surface to fill the undercuts. Finally, wet etching or dry etching is performed to etch back silicon oxide film 73 so that the upper surface of SOI layer 3 is exposed as shown in FIG. 145. In this case, wet etching applies less damage to the surface of SOI layer 3 than the dry etching. Even if the dry etching is performed, the problem can be prevented by forming oxidation after the dry etching. In this manner, SOI layer 3 having round corners can be formed, and also the SOI structure in which fixed charges so not exist at the interface between SOI layer 3 and buried oxide film 2 can be easily formed. Thereby, the SOI-MOSFET which can suppress generation of a parasitic transistor can be obtained. A silicon nitride film may be used instead of silicon oxide film 73.

Iwamatsu et al. teach in column 3, lines 55-67, and continuing to column 4, lines 1-33, that as shown in FIG. 211, an oxide film 120 is formed to cover nitride film 4a, side wall nitride film 4b, SOI layer 3 and buried oxide film 2. Anisotropic etching is effected on oxide film 120 to form side wall oxide films 120 as shown in FIG. 213. Thereafter, nitride film 4a, side wall nitride film 4b and oxide film 5 are removed. As shown in FIG. 214, gate oxide film 50 is formed over SOI layer 3 and side wall oxide film 120, and then

gate electrode 6 is formed on gate oxide film 50. In the structure thus formed, since side wall oxide film 120 is interposed between the side surface of SOI layer 3 and gate electrode 6, a portion of the parasitic transistor corresponding to a gate oxide film has a large thickness, so that an electric field applied from gate electrode 6 in the parasitic transistor is weaken. Consequently, the subthreshold characteristics of regular transistor is prevented from being affected by the characteristics of the parasitic transistor.

However, the proposed manufacturing process may suffer from the following problem. FIGS. 215 to 217 are cross sections showing the problem of the proposed manufacturing process. In the proposed manufacturing process, heat treatment is performed to activate the impurity implanted into SOI layer 3 after forming oxide film 120 at the step shown in FIG. 212. During this heat treatment, oxidant moves up to the bottom and upper surfaces of the side portion of SOI layer 3 as shown in FIG. 215. Thereby, the side portion of SOI layer 3 is shaped into an acute form. In this state, the side wall oxide film 120 is formed as shown in FIG. 216, and then gate oxide film 50 and gate electrode 6 are formed. In this case, an electric field concentrates at the side portion of SOI layer 3. As a result, the threshold voltage of parasitic transistor lowers, and thus the parasitic transistor tends to be turned on. Thereby, the subthreshold characteristics of regular transistor are adversely affected.

Iwamatsu et al. further teach in column 22, lines 26-37, that referring to FIGS. 47 and 48, a semiconductor device of a fourth embodiment is provided with thermal oxidation films 5a covering side surfaces of SOI layer 3. There are formed oxide films 16 which are in contact with side surfaces of thermal oxidation films 5a and cover end surfaces of concavities 2b in buried oxide film 2. Thereby, it is possible to prevent such a disadvantage that gate electrode 6 extends up to the lower surface of SOI layer 3 due to formation of gate electrode 6 at the end of concavity 2b during the manufacturing process. As a result, it is possible to prevent concentration of an electric field which may be caused by the above extension of gate electrode 6.

Iwamatsu et al. teach in column 23, lines 8-14, that the side surface of SOI layer 3 is oxidized by about 200 Å to form oxide film 5a, and then side wall oxide film 16 is formed in contact with the side surface of oxide film 5a and the upper surface of

concavity 2b as shown in FIG. 46, before forming gate electrode 6. Thereafter, gate oxide film 5 and gate electrode 6 are formed.

Iwamatsu et al. teach in column 23, lines 18-27, that referring to FIG. 49, a fifth embodiment differs from the fourth embodiment in FIG. 47 in that it is not provided with thermal oxidation films and side wall oxide films covering the side surfaces of SOI layer 3. Even in this structure, the side surfaces of SOI layer 3 have rounded upper portions, so that concentration of the electric field at the upper side portions can be effectively prevented. Consequently, the subthreshold characteristics of regular transistor are prevented from being adversely affected by the parasitic transistor.

Iwamatsu et al. teach in column 29, lines 66-67, and continuing to column 30, lines 1-6, that after oxidation of SOI layers 3, the oxide films are removed by wet etching. This etching removes buried oxide film 2 to some extent and thus forms a concavity. Side wall oxide films 5b which partially fill the concavity are formed in contact with side surfaces of SOI layers 3. Thereafter, the semiconductor device of the fourteenth embodiment is completed after the steps such as channel doping at SOI layers 3 and formation of the gate electrodes.

Iwamatsu et al teach in column 32, lines 31-60, that as shown in FIG. 118, SOI layers 152 which are isolated from each other and have a thickness of about 1000 Å are formed on support substrate 151 made of a silicon oxide film which is formed, e.g., by the SIMOX method. Since pad oxide films (not shown) are formed on SOI layers 152, concavities 151a are formed at support substrate 151 when removing the pad oxide films. If concavity 151a were filled with the gate electrode which will be formed later, the electric field would disadvantageously concentrate at the filled portion. In order to avoid this disadvantage, as shown in FIG. 119, side wall oxide films 191 made of silicon oxide films are, formed on side surfaces of SOI layers 152 and inner surface portions of concavities 151a.

When forming side wall oxide films 191, additional concavities 151b are formed at support substrate 151 due to over-etching. This may result in disadvantageous increase of the difference in level. In order to avoid this disadvantage, the concavities are filled as described below in the embodiment. As shown in FIG. 121, silicon oxide films 192 are formed on the upper surfaces of SOI layers 152, and then a polycrystalline silicon layer

193 having a thickness of about 1500 Å is formed over the whole surface. Polysilicon layer 193 is polished by the CMP method using silicon oxide films 192 as stopper layers. Thereby, a structure shown in FIG. 122 is obtained. After removing silicon oxide films 192, a gate oxide layer 194 having a thickness of about 100 Å is formed as shown in FIG. 123. A gate electrode layer 195 having a thickness of about 1500 Å is formed on gate oxide film 194.

Applicant, on the other hand, teaches on page 4, lines 5-13, that the semiconductor device is strained to increase the mobility of the electrons and holes in its channel region. In accordance with one embodiment, the combination of a mesa isolation structure and a silicided gate structure increases the hole mobility by causing the channel region to be under a compressive stress. In accordance with another embodiment, the combination of underetching the buried oxide of the mesa structure and wrapping a gate dielectric and a gate material around the underetched mesa structure increases the electron and hole mobilities by causing the channel region to be under tensile stress. In these embodiments, the silicide is preferably nickel silicide. The stress can be further increased by annealing the silicide at an elevated temperature.

Accordingly, applicant's claim 1 calls for, among other things, forming a mesa structure from the semiconductor substrate, wherein the mesa structure has a first surface and first and second sidewalls and forming a gate structure over the mesa structure, wherein the gate structure has a gate surface and first and second sides, and wherein first and second portions of the gate structure wrap around the first and second sides and are disposed on the first and second sidewalls, respectively. Applicant's claim 14 calls for, among other things, providing a semiconductor-on-insulator mesa isolation structure, the semiconductor-on-insulator mesa isolation structure having a top surface and first and second sidewalls, forming a gate dielectric material on the top surface and the first and second sidewalls, forming a gate on the gate dielectric material, wherein the gate and the gate dielectric material cooperate to form a gate structure having a top surface and gate sidewalls, and forming a semiconductor material on portions of the top surface of the mesa isolation structure adjacent to the first and second sidewalls of the mesa isolation structure, wherein the semiconductor material wraps around portions of the gate sidewalls. Applicant's claim 19 calls for, among other things, forming a gate structure on

the semiconductor substrate, the gate structure having a gate surface, first and second opposing gate sidewalls, and third and fourth opposing gate sidewalls, wherein forming the gate structure includes forming a second layer of dielectric material on a portion of the isolation sidewalls, forming a second layer of semiconductor material over a portion of the second layer of dielectric material, wherein the second layer of dielectric material and the second layer of semiconductor material wrap around the third and fourth opposing gate sidewalls, and forming silicide from the gate surface and the second layer of semiconductor material, wherein the silicide strains the semiconductor material of the semiconductor substrate. At least these elements of applicant's claims 1, 14, and 19 are not included in the relied on reference of Iwamatsu et al. Because all elements of applicant's claims 1, 14, and 19 are not included in the relied on reference of Iwamatsu et al., the relied on reference cannot anticipate applicant's claims 1, 14, and 19.

Claims 2-11 and 13 depend either directly or indirectly from claim 1 and are believed allowable over the relied on reference of Iwamatsu et al. for at least the same reasons as claim 1. Claim 3 further sets out that forming the gate structure includes forming a second layer of dielectric material over the first layer of dielectric material. Claim 4 further sets out that forming the first layer of dielectric material includes forming portions of the first layer of dielectric material over the first and second sidewalls, and wherein a portion of the first layer of dielectric material serves as the first portion of the gate structure and another portion of the first layer of dielectric material serves as the second portion of the gate structure. At least these elements of applicant's claims 3 and 4 are not included in the relied on reference of Iwamatsu et al., further precluding anticipation of claims 3 and 4.

Claims 15 and 16 depend from claim 14 and are believed allowable over the relied on reference of Iwamatsu et al. for at least the same reasons as claim 14. Claim 15 further sets out that providing the semiconductor-on-insulator mesa isolation structure includes forming portions of the first and second sidewalls to be below the top surface of the semiconductor-on-insulator mesa isolation structure. At least this element of applicant's claim 15 is not included in the relied on reference, further precluding anticipation of claim 15.

Claim 20 depends from claim 19 and is believed allowable over the relied on reference of Iwamatsu et al. for at least the same reasons as claim 19. Claim 20 further sets out forming the second layer of dielectric material on the portions of the first layer of semiconductor material adjacent the third and fourth opposing gate sidewalls. At least this element of applicant's claim 19 is not included in the relied on reference, further precluding anticipation of claim 19.

REJECTION OF CLAIMS 12, 17, AND 21-23 UNDER 35 U.S.C. § 103(a)

Claims 12, 17, and 21-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwamatsu et al., U.S. Patent No. 5,905,286 in view of Chen et al., Patent Application Publication 2004/0197969. This rejection is respectfully traversed.

Claim 12 depends indirectly from claim 1 and is believed allowable over the relied on references, either alone or in combination, for at least the same reasons as claim 1.

Claim 17 depends from claim 14 and is believed allowable over the relied on references, either alone or in combination, for at least the same reasons as claim 14.

Claims 21-23 depend indirectly from claim 19 and are believed allowable over the relied on references, either alone or in combination, for at least the same reasons as claim 19.

ALLOWABLE SUBJECT MATTER

Claims 18 and 24 were objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. The base claims and any intervening claims from which claims 18 and 24 depend are believed to be allowable. Accordingly, claims 18 and 24 are believed to be in condition for allowance.

CONCLUSION

No new matter is introduced by the amendments herein. Based on the foregoing, applicant believes that all claims under consideration are in condition for allowance. Reconsideration of this application is respectfully requested.

Respectfully submitted,

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